In the Claims:

Please amend the claims as follows:

1-12. (Cancelled).

13. (Currently Amended) A method of fabricating a ferroelectric memory device, the method comprising:

forming a lower insulating layer including a conductive plug on a semiconductor substrate;

forming an oxygen-diffusion barrier pattern that is electrically connected to the conductive plug and forming an upper insulating pattern on the lower insulating layer such that the upper insulating pattern surrounds sidewalls of the oxygen-diffusion barrier pattern and a top surface of the upper insulating pattern is higher than a top surface of the oxygen-diffusion barrier pattern;

forming a lower electrode layer on the upper insulating pattern and the oxygen-diffusion barrier pattern;

forming a ferroelectric layer on the lower electrode layer; ~~and~~

forming an upper electrode layer on the ferroelectric layer;

patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer; and

after forming the upper electrode layer, forming a third insulating layer that directly contacts sidewalls of the patterned lower electrode layer, the patterned ferroelectric layer and the patterned upper electrode layer.

14. (Original) The method of Claim 13, wherein the forming the oxygen-diffusion barrier pattern comprises:

forming a conductive oxygen-diffusion barrier layer and a hard mask layer on the lower insulating layer; and

patterning the hard mask layer and the conductive oxygen-diffusion barrier layer to be electrically connected to the contact plug.

15. (Original) The method of Claim 14, wherein forming the upper insulating pattern comprises:

forming an upper insulating layer on the lower insulating layer, the oxygen-diffusion barrier pattern and the hard mask pattern;

planarizingly etching the upper insulating layer using the hard mask pattern as a planarization stop to form the upper insulating pattern; and

selectively removing the hard mask pattern.

16. (Original) The method of Claim 15, wherein the hard mask layer is formed of a material having etch selectivity with respect to the upper insulating layer.

17. (Original) The method of Claim 15, wherein the hard mask layer is formed of a material including nitrogen.

18. (Original) The method of Claim 17, wherein the material including nitrogen comprises titanium nitride, silicon nitride or titanium aluminum nitride.

19. (Cancelled).

20. (Cancelled).

21. (Original) The method of Claim 13, wherein the oxygen-diffusion barrier pattern is a single layer pattern formed of iridium, ruthenium or osmium, a double layer pattern formed of sequentially stacked iridium and titanium aluminum nitride or a triple layer pattern formed of sequentially stacked iridium, titanium aluminum nitride and titanium.

22. (Original) The method of Claim 13, wherein the upper electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer, and

wherein the lower electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

23. (Original) The method of Claim 22, wherein the noble metal oxide electrode includes iridium oxide, ruthenium oxide, lanthanum strontium cobalt oxide (LSCO), yttrium barium cobalt oxide (YBCO) or lanthanum nickel oxide (LNO).

24. (Original) The method of Claim 22, wherein the noble metal comprises platinum, iridium, ruthenium, osmium, and lanthanum.

25. (Original) The method of Claim 13, wherein forming the ferroelectric layer comprises depositing the ferroelectric layer on the entire surface of the lower electrode layer.

26. (Currently Amended) A method of forming a ferroelectric memory device comprising:

forming a lower insulating layer including a contact plug on a semiconductor substrate;

forming an upper insulating layer on the lower insulting layer;

patterning the upper insulating layer to form an opening exposing the conductive plug ~~and the lower insulating layer~~;

forming an oxygen-diffusion barrier pattern in the opening such that a top surface of the oxygen-diffusion barrier pattern is lower than a top surface of the upper insulating layer;

conformally forming a lower electrode layer directly on both an upper surface of the upper insulating layer and ~~on~~ an upper surface of the oxygen-diffusion barrier pattern;

forming a ferroelectric layer on the lower electrode layer;

forming an upper electrode layer on the ferroelectric layer; and then

patterning the upper electrode layer, the ferroelectric layer and the lower electrode layer.

27. (Original) The method of Claim 26, wherein the oxygen-diffusion barrier pattern is a single layer pattern formed of iridium, ruthenium or osmium, a double layer pattern formed of sequentially stacked iridium and titanium aluminum nitride or a triple layer pattern formed of sequentially stacked iridium, titanium aluminum nitride and titanium.

28. (Original) The method of Claim 26, wherein the lower electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer, and wherein the upper electrode comprises a single layer electrode formed of a noble metal or a conductive noble metal oxide or a multi-layer electrode formed of a noble metal layer and a conductive noble metal oxide layer.

29. (New) The method of Claim 13, wherein the ferroelectric layer is deposited directly on only the lower electrode layer.

30. (New) The method of Claim 13, wherein the lower electrode layer is a single layer lower electrode layer that is in direct contact with both the oxygen diffusion barrier pattern and with the ferroelectric layer.

31. (New) The method of Claim 13, further comprising:

forming a transistor at the semiconductor substrate;

forming a first interlayer insulating layer on the semiconductor substrate and on the transistor;

forming an opening in the first interlayer insulating layer to expose a source/drain region of the transistor;

forming a conductive material in the opening to form a capacitor contact pad; and

wherein the conductive plug is formed to be in electrical contact with the capacitor contact pad.

32. (New) The method of Claim 33, wherein forming a lower insulating layer including a conductive plug on a semiconductor substrate comprises:

forming the lower insulating layer on the first interlayer insulating layer and on the capacitor contact pad;

patterning the lower insulating layer to form a contact hole that exposes a top surface of the capacitor contact pad; and

forming the conductive plug in the contact hole.

33. (New) The method of Claim 26, wherein forming the oxygen-diffusion barrier pattern comprises:

forming an oxygen-diffusion barrier layer in the opening; and

etching a portion of the oxygen-diffusion barrier layer filling the opening.

34. (New) The method of Claim 26, wherein the ferroelectric layer is deposited directly on only the lower electrode layer.

35. (New) The method of Claim 34, wherein the lower electrode layer is a single layer lower electrode layer that is in direct contact with both the oxygen diffusion barrier pattern and with the ferroelectric layer.

36. (New) The method of Claim 26, further comprising:

forming a transistor at the semiconductor substrate;

forming a first interlayer insulating layer on the semiconductor substrate and on the transistor;

forming an opening in the first interlayer insulating layer to expose a source/drain region of the transistor;

forming a conductive material in the opening to form a capacitor contact pad; and

wherein the conductive plug is formed to be in electrical contact with the capacitor contact pad.

37. (New) The method of Claim 36, wherein forming a lower insulating layer including a conductive plug on a semiconductor substrate comprises:

forming the lower insulating layer on the first interlayer insulating layer and on the capacitor contact pad;

patterning the lower insulating layer to form a contact hole that exposes a top surface of the capacitor contact pad; and

forming the conductive plug in the contact hole.

38. (New) The method of Claim 26, further comprising forming a third insulating layer that directly contacts sidewalls of the patterned lower electrode layer, the patterned ferroelectric layer and the patterned upper electrode layer.

39. (New) A method of fabricating a ferroelectric memory device, the method comprising:

forming a lower insulating layer including a conductive plug on a semiconductor substrate;

forming an oxygen-diffusion barrier layer that is electrically connected to the conductive plug, wherein the oxygen-diffusion barrier pattern is a single layer pattern formed of iridium, ruthenium or osmium, a double layer pattern formed of sequentially stacked iridium and titanium aluminum nitride or a triple layer pattern formed of sequentially stacked iridium, titanium aluminum nitride and titanium;

forming a hard mask layer directly on the oxygen-diffusion barrier layer;

patterning the hard mask layer and the oxygen-diffusion barrier layer to provide a hard mask pattern and an oxygen diffusion barrier pattern such that the oxygen diffusion barrier pattern is electrically connected to the conductive plug;

forming an upper insulating pattern on the lower insulating layer such that the upper insulating pattern surrounds sidewalls of the oxygen-diffusion barrier pattern and a top surface of the upper insulating pattern is higher than a top surface of the oxygen-diffusion barrier pattern;

removing the hard mask pattern;

forming a lower electrode layer on the upper insulating pattern and the oxygen-diffusion barrier pattern;

forming a ferroelectric layer on the lower electrode layer; and

forming an upper electrode layer on the ferroelectric layer.

40. (New) The method of Claim 39, further comprising:

patterning the lower electrode layer, the ferroelectric layer and the upper electrode layer; and

after forming the upper electrode layer, forming a third insulating layer that directly contacts sidewalls of the patterned lower electrode layer, the patterned ferroelectric layer and the patterned upper electrode layer.

41. (New) The method of Claim 40, wherein forming a lower electrode layer on the upper insulating pattern and the oxygen-diffusion barrier pattern comprises conformally forming a lower electrode layer directly on both an upper surface of the upper insulating layer and an upper surface of the oxygen-diffusion barrier pattern.

42. (New) The method of Claim 41, wherein the ferroelectric layer is deposited directly on only the lower electrode layer.